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EXAMINER
MUTSCHLER, BRIAN L

ART UNIT	PAPER NUMBER
1753	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

A3-3

Office Action Summary	Application No.	Applicant(s)	
	10/008,665	ALLING ET AL.	
	Examiner	Art Unit	
	Brian L. Mutschler	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-31 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Comments

1. The relative limitations, such as "distinct from" and "substantially" have been interpreted in light of the accompanying definitions of the terms in the present disclosure. In claims 1, 11 and 21, the limitation "a second reduction potential distinct from the first reduction potential" is considered to be at least a 0.1 V potential difference, as defined on page 7 of the disclosure. In claims 2, 12 and 25, the definition of a "substantially homogenous" material is understood to be a material that is at least 90% pure, as disclosed on page 4. In claims 8, 18 and 30, the definition of "the second metal layer is substantially less conductive than the first [metal] layer" is understood to mean that the second metal layer has a resistance that is at least 10% higher than the first metal layer, as defined on page 7 of the present disclosure.

2. The limitation recited in claim 10, wherein "the substrate is a lead of a semiconductor device, or an interconnect of a semiconductor device" appears to be incorrect. Is the substrate performing the function of the lead or interconnect, or is the first metal layer performing the function?

Specification

3. The disclosure is objected to because of the following informalities:

   a. In line 6 of the last paragraph on page 4, please change "ships" to --chips--.

   Appropriate correction is required.

Claim Objections

4. Claims 8, 18, 21 and 30 are objected to because of the following informalities:

   a. In claim 8 at line 2, please insert --metal-- after "first";

   b. In claim 18 at line 2, please insert --metal-- after "first";

   c. In claim 21 at line 6, the second occurrence of "layer" should be deleted; and

   d. In claim 30 at line 2, please insert --metal-- after "first".

   Appropriate correction is required.

5. Claim 30 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend from itself. Claim 30 depends from "any one of claims 21 through 30". See MPEP § 608.01(n). Accordingly, the claim has not been further treated on the merits.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 1-31 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for depositing multiple metal layers using a single bath, does not reasonably provide enablement for plating multiple layers using separate

baths, which is within the scope of the claims. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims.

The present disclosure describes a method for electrolytically depositing a first metal layer and a second metal layer, wherein both metal layers are plated using a single bath. However, the claims are open to having separate plating baths. While an plating composition comprising a copper metal source and a second metal source is recited, the composition could be using for the deposition of a copper alloy, and a second composition could also be used to plate another layer. The disclosure does not provide enablement for such a use, and therefore, the claims should be amended to claim that which is enabled by the disclosure, i.e., that both metal layers are deposited using the same plating composition. A preferred way to amend the claims would also indicate that the first metal layer of copper (or the first metal layer, as recited in claim 21) is formed the copper metal source (or the first metal source) of the plating composition, and the second metal layer is formed by the second metal source of the plating composition. This would identify that the same plating solution is used for the deposition of both layers and also identify that the sources of metal are actually used in the deposition of the layers.

Tadokoro et al. (U.S. Pat. No. 4,108,739) disclose a method for plating an electronic device with multiple distinct metal layers from a single bath and also disclose the prior art technique, which requires a plurality of separate plating solutions to create the desired layers (see col. 1, lines 19-56 for the prior art technique). As can be seen

from the disclosure of Tadokoro et al., the multiple bath technique requires a plurality of steps to overcome the deficiencies associated with the multiple bath process, such as providing a plurality of plating baths, transferring the substrate from one bath to another, and a washing step to prevent intermixing of the plating solutions. These important steps are not disclosed in the present application.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 11-16, 18, 20, 21, 27, 28, 30 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Meltzer et al. (U.S. Pat. No. 6,547,946), with evidence of physical properties provided by CRC Handbook of Chemistry and Physics ("Thermal and Physical Properties of Pure Metals", 3rd Electronic Edition).

Regarding claims 11, 21 and 31, Meltzer et al. disclose a method for depositing multiple metal layers on a printed wiring board by single bath deposition, wherein a copper layer and a nickel layer are plated from a single bath containing a copper metal source and a nickel metal source (fig. 1; col. 5, lines 8-52). Copper is plated using a low

reduction potential and nickel is plated using a high reduction potential (fig. 3; col. 5, lines 8-28).

Regarding claim 12, the copper layer is formed as a homogenous layer (col. 5, lines 29-31).

Regarding claims 13-15 and 27, Meltzer et al. disclose that the nickel layer "contains a percentage of copper", which means the nickel layer is actually an alloy of nickel and copper (col. 5, lines 35-37).

Regarding claims 16 and 28, the reduction potentials used in the process of Meltzer et al. differ by at least 0.2 V (fig. 3).

Regarding claims 18 and 30, as seen in the table "Thermal and Physical Properties of Pure Metals", in the CRC Handbook of Chemistry and Physics, the resistivity of nickel is over 400% greater than the resistivity of copper. Therefore, any alloy comprising nickel with a percentage of copper would be expected to have a conductivity substantially less than that of copper.

Regarding claim 20, Meltzer et al. disclose that solder is deposited on the substrate (col. 5, lines 32-35).

Regarding claim 31, the metal layers are deposited from the same plating bath (col. 5, lines 29-52).

Since Meltzer et al. teach the method limitations recited in the instant claims, the reference is deemed to be anticipatory.

10. Claims 21, 25-27, 29 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Cohen (U.S. Pat. No. 4,923,574).

Regarding claim 21, Cohen discloses a method for depositing a plurality of metal layers on a substrate for making a record member (electronic device), comprises the steps of forming an overcoat consisting of tin and also forming a plurality of layers having metal rich layers alternating with layers of an alloy of that metal formed by modulating the current density or cathode potential (col. 3, line 51 to col. 4, line 9).

Regarding claim 25, Cohen discloses that the overcoat consists of tin (col. 3, lines 21-55).

Regarding claims 26 and 27, Cohen discloses that the overcoat may comprise an alloy of tin and antimony, bismuth, thallium or copper (col. 3, lines 55-58).

Regarding claim 29, Cohen discloses that the overcoat comprises a plurality of layers with layers of richer metal are alternated with layers of alloys of that metal (co. 3, line 67 to col. 4, line 1).

Regarding claim 31, Cohen teaches that a single plating bath is used and the layers are formed only by modulating the current density or potential (col. 4, lines 14-17).

Since Cohen teaches the method limitations recited in the instant claims, the reference is deemed to be anticipatory.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1-10 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meltzer et al. (U.S. Pat. No. 6,547,946) in view of Akram et al. (U.S. Pat. No. 5,893,966), with evidence of physical properties provided by CRC Handbook of Chemistry and Physics ("Thermal and Physical Properties of Pure Metals", 3rd Electronic Edition).

Meltzer et al. teach a method for making a printed wiring board having the limitations recited in claims 11-16, 18, 20, 21, 27, 28, 30 and 31 of the instant invention, as explained above in section 9.

Regarding claim 1, Meltzer et al. disclose a method for depositing multiple metal layers on a printed wiring board by single bath deposition, wherein a copper layer and a nickel layer are plated from a single bath containing a copper metal source and a nickel metal source (fig. 1; col. 5, lines 8-52). Copper is plated using a low reduction potential and nickel is plated using a high reduction potential (fig. 3; col. 5, lines 8-28).

Regarding claim 2, the copper layer is formed as a homogenous layer (col. 5, lines 29-31).

Regarding claims 3-5, Meltzer et al. disclose that the nickel layer "contains a percentage of copper", which means the nickel layer is actually an alloy of nickel and copper (col. 5, lines 35-37).

Regarding claim 6, the reduction potentials used in the process of Meltzer et al. differ by at least 0.2 V (fig. 3).

Regarding claim 7, Meltzer et al. disclose that the method for fabricating the layered printed wiring board was "adapted from layered electroforming techniques used to build up copper-nickel composite materials of high tensile strength [and t]hese materials typically had many alternating, very thin layers of each metal" (col. 5, lines 55-59).

Regarding claims 8 and 9, as seen in the table "Thermal and Physical Properties of Pure Metals", in the CRC Handbook of Chemistry and Physics, the resistivity of nickel is over 400% greater than the resistivity of copper. Therefore, any alloy comprising nickel with a percentage of copper would be expected to have a conductivity substantially less than that of copper.

The method of Meltzer et al. differs from the instant invention because Meltzer et al. do not disclose the following:

a. The substrate is a semiconductor substrate, as recited in claims 1 and 21;

b. A plurality of first metal layers are deposited with a plurality of alternating second metal layers, as recited in claim 7;

c. The first metal layer functions as an electrical circuit and the second metal layer functions as an insulator layer, as recited in claim 9;

d. The substrate is a lead or interconnect of a semiconductor device, as recited in claim 10;

e. The substrate is a semiconductor package substrate, as recited in claim 23; and

f. The substrate is a multi-chip module, chip capacitor, chip resistor, lead frame or an opto-electronic device, as recited in claim 24.

Regarding claims 1 and 21-24, Akram et al. teach, "Semiconductor wafers, substrates and printed circuit boards (collectively hereinafter 'semiconductor substrates') are often coated with various metals" (col. 1, lines 16-20). Furthermore, Akram et al. teach, "Techniques for coating semiconductor substrates include electrodeposition...[and e]lectrodeposition has become a commonly used technology" (col. 1, lines 21-24).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the substrate used in the method of Meltzer et al. to use a semiconductor substrate because Akram et al. teach that semiconductor substrates are commonly coated using electrodeposition techniques and that semiconductors include semiconductor wafers, substrates and printed circuit boards. Regarding the different types of semiconductor substrates recited in claims 23 and 24, such semiconductors are common semiconductor types and it would have been obvious to one skilled in the art to form electrochemical deposits on such semiconductors because the methods and results are equivalent.

Regarding claim 7, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Meltzer et al. to plate a plurality of alternating layers because Meltzer et al. teach that he method is adapted from a method used to plate such a plurality of layers and that a material comprising such a plurality of layers has a high tensile strength.

Regarding claims 9 and 10, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the device fabricated by the method of Meltzer et al. to have the first metal layer function as an electrical circuit and the second metal layer function as an insulator layer or having the substrate (first metal layer?) function as a lead or interconnect because the structure of the device formed in the method of Meltzer et al. is identical to the structure of the device formed in the method recited in the instant claims, and therefore, the layers would be expected to function or be capable of functioning in a similar manner to the claimed function.

13. Claims 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meltzer et al. (U.S. Pat. No. 6,547,946), with evidence of physical properties provided by CRC Handbook of Chemistry and Physics ("Thermal and Physical Properties of Pure Metals", 3rd Electronic Edition).

Meltzer et al. teach a method for making a printed wiring board having the limitations recited in claims 11-16, 18, 20, 21, 27, 28, 30 and 31 of the instant invention, as explained above in section 9.

Regarding claim 17, Meltzer et al. disclose that the method for fabricating the layered printed wiring board was "adapted from layered electroforming techniques used to build up copper-nickel composite materials of high tensile strength [and t]hese materials typically had many alternating, very thin layers of each metal" (col. 5, lines 55-59).

Regarding claim 19, as seen in the table "Thermal and Physical Properties of Pure Metals", in the CRC Handbook of Chemistry and Physics, the resistivity of nickel is over 400% greater than the resistivity of copper. Therefore, any alloy comprising nickel with a percentage of copper would be expected to have a conductivity substantially less than that of copper.

The method of Meltzer et al. differs from the instant invention because Meltzer et al. do not disclose the following:

a. A plurality of first metal layers are deposited with a plurality of alternating second metal layers, as recited in claim 17; and

b. The first metal layer functions as an electrical circuit and the second metal layer functions as an insulator layer, as recited in claim 19.

Regarding claim 17, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Meltzer et al.

to plate a plurality of alternating layers because Meltzer et al. teach that he method is adapted from a method used to plate such a plurality of layers and that a material comprising such a plurality of layers has a high tensile strength.

Regarding claim 19, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the device fabricated by the method of Meltzer et al. to have the first metal layer function as an electrical circuit and the second metal layer function as an insulator layer because the structure of the device formed in the method of Meltzer et al. is identical to the structure of the device formed in the method recited in the instant claims, and therefore, the layers would be expected to function or be capable of functioning in a similar manner to the claimed function.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references teach methods for forming multiple metal layers from a single bath:

U.S. Pat. No. 4,108,739	Tadokoro et al.
U.S. Pat. No. 4,869,971	Nee et al.
U.S. Pat. No. 5,156,729	Mahrus et al.
U.S. Pat. No. 5,320,719	Lasbmore et al.
U.S. Pat. No. 6,344,124	Bhatnagar

Cohen et al., "Electroplating of Cyclic Multilayered Alloy (CMA) Coatings", *J. Electrochem. Soc.* 130 (10), (1983), pp. 1987-1995.

Zue et al., "The electrodeposition of a copper/nickel multilayer alloy on beryllium bronze substrate", *J. Phys. D: Appl. Phys.* 30, (1997), pp. 3301-3306.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian L. Mutschler whose telephone number is (703) 305-0180. The examiner can normally be reached on Monday-Friday from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on (703) 308-3322. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9310 for regular communications and (703) 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0661.

NAM NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700

blm
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